

Appl. No. 10/064,972
Amdt. dated March 28, 2006
Reply to Office action of January 03, 2006

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig.2 and Fig.3. These sheets, which include Fig.2 and Fig.3, replace the original sheets including Fig.2 and Fig.3. In Fig.2, element 52 has been labeled "Control Circuit" as required by the Examiner. In Fig.3, the two voltage sources previously labeled as "PBIAS" have been relabeled "BIAS" and element 92 has been labeled "PBIAS". Additionally, in Fig.3, transistors 82, 84, and 86 have been changed from inverted transistors to transistors.

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Attachment:

Replacement Sheet

2 pages

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REMARKS/ARGUMENTS

This is a full and timely response to the Office action of January 3, 2006. In this response, the drawings, specification, and claims have been amended as required by the Examiner. Additionally, Fig.3 has been slightly amended to agree with the written specification. Independent claims 1 and 9 have been amended to include limitations not found in known prior art. Claim 7 has been cancelled. Reconsideration of the drawings, specification, and all claims pending in the application is respectfully requested.

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1. Drawings

10 Fig.2 has been amended by labeling element 52 a "Control Circuit" as required by the Examiner.

15 Additionally, Fig.3 has been amended so that the two voltage sources previously labeled as "PBIAS" have been relabeled "BIAS" and element 96 has been labeled "PBIAS". Because the Examiner has stated possible ambiguity regarding the control circuit 80 (Fig.3) and the control circuit 50 (Fig.2), these changes have been made to more clearly point out the present invention.

20 Paragraph [0021] as filed states "The control circuit 80 comprises transistors 92, 94, inverted transistors 82, 84, 86, 88, 90, three current sources 11, 12, 13, a ground 96, and an electrical bias PBIAS. In this example, the ground 96 is to be used as a bias for the driver circuit 50."

25 Thus, the "PBIAS" in Fig.3 is not the same thing as the "PBIAS" in Fig.2. Because the PBIAS in Fig.2 is used as a bias for the driver circuit (Paragraph [0019]) and in Fig.3, the ground 96 is to be used as a bias for the driver circuit (Paragraph [0021]), the ground 96 in Fig.3 is functionally the same as the "PBIAS" in Fig.2. Therefore, the ground 96 has been labeled as "PBIAS" for uniformity. However, because the control circuit 80 also inputs a bias previously also labeled "PBIAS" (Paragraph [0021]), the inputted bias has been relabeled as "BIAS" to avoid confusion. Minor amendments reflecting this terminology have also been

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made to the relevant paragraphs [0019] and [0021], again for uniformity. Additionally, transistors 82, 84, and 86 have been changed from inverted transistors to transistors. No limitation on the type of transistor used for 82, 84, and 86 is found in the specification, and Paragraph [0022] clearly defines functioning of the control circuit 80. The change of 5 transistor types is therefore supported by the specification, not limiting, and merely makes the drawings correspond to the written description as required by the Examiner and should be allowable. No new material has been introduced.

Acceptance and reconsideration of the drawings is respectfully requested.

10 **2. Specification**

A replacement Abstract as identified at the end of the "Amendments to the Specification" section is included with this response. Reconsideration of the replacement Abstract is respectfully requested.

15 Typographical errors that inadvertently occurred during electronic filing of this application and pointed out by the Examiner in Paragraphs [0004], [0006], [0007], [0019], and [0023] have been corrected. Other Examiner cited errors in Paragraphs [0019] and [0021] have also been corrected. As noted previously in this response, Fig.3 has been slightly amended so that the cited discussion of the control 80 in Paragraph [0022] is believed to accurately correspond with Fig.3 as required. No new material has been introduced.

20 Reconsideration of the specification is respectfully requested.

3. Claim Objections

Amendments have been made to correct Examiner cited informalities in claims 5-6, and 9-12. Claim 7 has been cancelled.

25 Reconsideration of claims 5-6 and 9-12 under the informalities objection is respectfully requested.

4. Claim Rejections 35 U.S.C. 112

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Regarding First Paragraph rejections of claims 1-12

As previously mentioned and supported in the discussion about Drawings in this response, Fig.3 has been slightly amended by changing the labeling of various elements including "PBIAS" and "BIAS" to clear up any possible ambiguity in the teachings of the 5 invention. The control circuit 80 receives and utilizes BIAS to generate and output the PBIAS referred to in Fig.2. According to the present invention, the generated PBIAS (96 in Fig.3) is generated by the summation of one or more currents. The selection of which currents to sum when generating PBIAS is done according to at least one control indicator as discussed in Paragraphs [0022] and [0023].

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Regarding the number of control indicators used, referring to Fig.3, Paragraph [0021] clearly states:

"It is obvious that a single control indicator can be used to select between [[to]] two outputted current levels and the present invention is not to be limited by the number of 15 control indicators used. In this example, four control indicators are used for convenience to illustrate a useful application of the present invention."

Paragraph [0020] further confirms this with:

"It is understood that there are numerous ways to implement a control circuit for the present invention and FIG. 3 is merely an illustration of only one possible control circuit. 20 The spirit of the present invention applies to any method of using one or more control indicators to combine one or more current sources and output the combined current to be used as an electrical bias for a differential signal driver."

Thus, with the modifications to Fig.3, the Applicant believes that the inventive concept of using control indicators to selectively sum currents with the summed currents used as a 25 bias for the differential signal driver is taught at a level where one skilled in the art would be able to build and operate the instant device. For example, one skilled in the art would easily recognize, when taught how to generate the PBIAS according to the present invention, how to additionally generate the corresponding NBIAS shown in Fig.2. While circuitry is not to be

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limited to the example illustrated in Fig.3, Fig.3 is included with this application to conform with the enablement requirement by teaching one possible way that the present invention can be accomplished. Reconsideration of claims 1-12 under 35 U.S.C. 112, first paragraph is respectfully requested.

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Regarding Second Paragraph rejections of claims 5-7 and 10-12

Claims 5 and 6 have been slightly amended to correct for the cited lacking antecedent basis. Claim 7 has been cancelled.

10 The Applicant respectfully disagrees with this rejection of claims 10-12 inasmuch as they appear to add additional limitations to claim 9. However, in an effort to cooperate with the Examiner to the maximum extent and without giving up any future rights whatsoever concerning the subject matter of claims 10-12 as filed, claims 10-12 have been amended in this response merely in an attempt to insure that the Examiner considers the application in allowable form.

15 Reconsideration of claims 5-6 and 10-12 under 35 U.S.C. 112 is respectfully requested.

5. Claim Rejections 35 U.S.C. 102(e)

20 Col.5, lines 50-61 of Chow state "With reference to FIG. 6, there are 4 control lines: R, L, M, and B, which select the standards RSDS, LVDS, mini-LVDS, and BLVDS respectively. A standard is selected by pulling the control line for the selected standard high. The remaining control lines must remain low. ... As an example, assume R is pulled high. This switches on the nmos transistor 610, which places the reference voltage of the selected voltage source 613 (1.3V) at the negative terminal of the operational amplifier 630."

25 Chow teaches providing a plurality of voltage sources, of which one is selected to provide the voltage source for generating the bias. The remaining voltage sources of the plurality of voltage sources are not utilized because "the remaining control lines must be kept low" as clearly taught in the above-cited paragraph. Chow does utilize current

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mirrors and the like for various reasons during generation of the bias, but utilizes a one-to-one relationship between current sources and outputted bias levels.

Both independent claims 1 and 9 have been amended to include the limitations that the control circuit selects a plurality of current sources according to the control indicator and that

5 the outputted bias is generated by summing the currents from the selected sources. These limitations are clearly supported as base concepts of the present invention by Paragraphs [0020] and [0022] as filed. No new material has been introduced.

Obviously, there are structural and functional differences between having a plurality of voltages sources, each of which is used independently according to a control signal to

10 generate a bias as does Chow, and a plurality of voltage sources which are selectively chosen according to a control signal and summed to generate a bias as is taught and claimed by the instant invention. A real world advantage of the teachings of the instant invention is that a fewer number of voltage sources can be used to generate a larger number of different bias currents through the summation of selected voltage sources, while a device of Chow requires

15 a one-to-one relationship between voltage sources and outputted bias levels. The present invention decreases cost and increase flexibility.

Reconsideration of claims 1-6 and 8-12 under the 35 U.S.C. 102 rejection is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

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Sincerely yours,

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